**LISTING OF THE CLAIMS**:

Claim 1 (Currently Amended) A selective silicon-on-insulator (SOI) structure comprising:

a silicon-on-insulator (SOI) substrate material comprising a top Si-containing layer having a plurality of SOI devices located thereon, said SOI devices are in contact with an underlying Si-containing substrate via a body contact region; and

a DC node diffusion region adjacent to one of said SOI devices, said DC node diffusion region is located within bulk silicon without oxide underneath thereby the DC node diffusion region is in contact with said Si-containing substrate.

Claim 2 (Original) The selective SOI structure of Claim 1 wherein said plurality of SOI devices comprise metal oxide semiconductor field effect transistors (MOSFETs).

Claim 3 (Original) The selective SOI structure of Claim 1 wherein said plurality of SOI devices are located atop a top Si-containing layer of said SOI substrate material.

Claim 4 (Original) The selective SOI structure of Claim 3 wherein said plurality of SOI devices comprising active source/drain regions located with said top Si-containing layer.

Claim 5 (Original) The selective SOI structure of Claim 4 wherein said active source/drain regions are located atop a buried oxide.

Claim 6 (Currently Amended) The selective SOI structure of Claim [[4]] 5 wherein said buried oxide is a lateral etched area located adjacent to a trench isolation region.

Claim 7 (Original) Thee selective SOI structure of Claim 1 wherein said DC node diffusion region comprises a region in which a source voltage can be applied, a region in which a reference voltage can be applied, a ground region or any combination.

Claim 8 (Cancelled)

Claim 9 (Original) The selective SOI structure of Claim 2 wherein the MOSFETs comprise a gate dielectric and a gate conductor.

Claim 10 (Original) The selective SOI structure of Claim 1 wherein said SOI substrate is an additive SOI substrate having discriminative regions for forming said DC node diffusion region.

Claim 11 (Original) The selective SOI structure of Claim 1 wherein said SOI substrate is comprised of a Si-containing material.

Claim 12 (Original) The selective SOI structure of Claim 11 wherein said Si-containing material is selected from the group consisting of Si, SiGe, SiC, SiGeC, Si/Si, Si/SiC, and Si/SiGeC

Claim 13 (Original) The selective SOI structure of Claim 3 wherein said top Si-containing layer has a thickness from about 50 to about 200 nm.

Claim 14 (Currently Amended) An integrated circuit comprising at least one selective silicon-on-insulator (SOI) structure said at least one selective SOI structure comprising a silicon-on-insulator (SOI) substrate material comprising a top Si-containing layer having a plurality of SOI devices located thereon, said SOI devices are in contact with an underlying Si-containing substrate via a body contact region; and a DC node diffusion region adjacent to one of said SOI devices, said DC node diffusion region <u>is located within bulk silicon without oxide underneath thereby the DC node diffusion region</u> is in contact with said Si-containing substrate.

Claim 15 (Currently Amended) A semiconductor substrate comprising:

an SOI substrate;

a DC node diffusion region in said SOI substrate; and

a buried oxide material within said SOI substrate, wherein said DC node diffusion region is located within bulk silicon without oxide underneath thereby the DC node diffusion region is in contact with an underlying Si-containing substrate of said SOI substrate.

Claim 16 (Original) The semiconductor substrate of Claim 15 wherein said SOI substrate includes a top Si-containing layer.

Claim 17 (Original) The semiconductor substrate of Claim 16 wherein the top Si-containing layer and the underlying Si-containing substrate are composed of a silicon semiconductor material selected from the group consisting of Si, SiGe, SiC, SiGeC, Si/Si, Si/SiC, and Si/SiGeC

Claim 18 (Original) The semiconductor substrate of Claim 16 wherein said top Si-containing layer has a thickness from about 50 to about 200 nm.

Claim 19 (Original) The semiconductor substrate of Claim 15 wherein the buried oxide material is crystalline.

Claim 20 (Original) The semiconductor substrate of Claim 15 wherein the buried oxide material is non-crystalline.

Claim 21 (Original) The semiconductor substrate of Claim 15 wherein the buried oxide material has a thickness from about 30 to about 100 nm.

Claim 22 (Original) The semiconductor substrate of Claim 15 further comprising at least one trench isolation region that is in contact with said buried oxide material.

Claim 23 (Original) The semiconductor substrate of Claim 15 wherein said DC node diffusion region comprises a region in which a source voltage can be applied, a region in which a reference voltage can be applied, a ground region or any combination.

Claim 24 (Cancelled)